Claims

1.-11. (cancelled)

12. (new) A method for handling digital sound sequences in a telecommunications system having a CPU, a working memory for the CPU, and a switching network, the method comprising:

establishing connections to a telecommunication terminal via the switching network by the telecommunications system;

outputting sound sequences via the switching network to the telecommunications terminal by the telecommunications system; and

using at least a part of the working memory to store the digital sound sequences.

13. (new) The method as claimed in the preceding claim 12, wherein the CPU performs a data transfer of the digitally stored sound sequences between the working memory and switching network.

14. (new) The method as claimed in the preceding claim 12, wherein data is transferred packet by packet and a time slot assigner (TSA) is used between the working memory and the switching to assign the digital sound sequences to programmed timeslots.

15. (new) The method as claimed in the preceding claim 13, wherein data is transferred packet by packet and a time slot assigner (TSA) is used between the working memory and the switching to assign the digital sound sequences to programmed timeslots.

16. (new) The method as claimed in the preceding claim 14, wherein a FIFO shift register is used in the time slot assigner (TSA) to support a packet-by-packet data transfer of the digital sound sequences.

17. (new) The method as claimed in the preceding claim 15, wherein a FIFO shift register is used in the time slot assigner (TSA) to support a packet-by-packet data transfer of the digital sound sequences.

18. (new) The method as claimed in the preceding claim 12, wherein in order to unload the CPU a microcontroller is used between the working memory and a time slot assigner (TSA), wherein the microcontroller is initialized by the CPU to perform the transfer of the digital sound sequences.

19. (new) The method as claimed in the preceding claim 18, wherein the microcontroller is a Direct Memory Access (DMA) controller.

20. (new) The method as claimed in the preceding claim 13, wherein in order to unload the CPU a microcontroller is used between the working memory and a time slot assigner (TSA), wherein the microcontroller is initialized by the CPU to perform the transfer of the digital sound sequences.

21. (new) The method as claimed in the preceding claim 18, wherein the CPU requests the microcontroller to set the start address of the digital sound sequences in the working memory and to set the destination address in the FIFO shift register

of the time slot assigner (TSA) in order to play back the digital sound sequences.

22. (new) The method as claimed in the preceding claim 18, wherein the CPU requests the microcontroller to set the start address of the digital sound sequences in the FIFO shift register of the time slot assigner (TSA) and to set the destination address in the working memory for recording sound sequences.

23. (new) The method as claimed in the preceding claim 21, wherein the CPU requests the microcontroller to set the start address of the digital sound sequences in the FIFO shift register of the time slot assigner (TSA) and to set the destination address in the working memory for recording sound sequences.

24. (new) The method as claimed in the preceding claim 12, further comprising:

digitizing sound sequences and storing the digitized sound sequences in the working memory by the telecommunications system.

25. (new) The method as claimed in the preceding claim 12, wherein at a certain filling level of the FIFO shift register, the time slot assigner (TSA) requests the CPU by an interrupt command to start or to stop a new data transfer.

26. (new) The method as claimed in the preceding claim 12, wherein in order to unload the CPU a CPU with integrated

Peripheral Exchange Control (PECC) transfer feature is used between the working memory and a time slot assigner (TSA).

27. (new) The method as claimed in the preceding claim 12, wherein the digital sound sequences are MOH (= Music on Hold), voice sequences, or signal tones.

28. (new) The method as claimed in the preceding claim 12, wherein program code and/or data of telecommunications subscribers being stored in the working memory.

29. (new) A method for handling digitally stored sound sequences in a telecommunications system having a CPU, a working memory for the CPU, and a switching network, the method comprising:

setting up connections to telecommunications terminals via the switching network by the telecommunications system; and

outputting sound sequences via the switching network to at least one telecommunications terminal, wherein

at least a part of the working memory is used to store the digitally stored sound sequences.

30. (new) A telecommunications system, comprising:

a CPU having a working memory; and

a switching network for connecting a terminal; and

mechanisms for performing the method as claimed in claim 12.

31. (new) The telecommunications system according to claim 30, wherein the mechanisms

for performing the method as claimed in claim 12 are program mechanisms and/or program modules.